NVM Express Technical Errata

Errata ID	**029**
Change Date	**6/5/2012**
Affected Spec Ver.	**NVM Express 1.0c**
Corrected Spec Ver.	

Submission info

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A recommendation is added to the Compare and Write section to ensure data integrity is preserved. Specifically, hosts should issue Compare and Write commands for a size less than or equal to the atomic write unit. NVMe devices may choose to fail Compare and Write requests for sizes larger than an atomic write unit.

The single and multiple message MSI behavior inaccurately describes the message action when some bits, but not all bits, are cleared in the IS register. This erratum describes that a new message shall be sent in this case.

The Offset (OFST) field for the Firmware Image Download command is clarified to be the number of Dwords.

Corrections are made to section 5.12 to correctly identify Features that are optional vs mandatory.

Description of the specification technical flaw:

Modify section 6.2.1 as shown below:

The Compare and Write fused operation compares the contents of the logical block(s) specified in the Compare command to the data stored at the indicated LBA range. If the compare is successful, then the LBA range is updated with the data provided in the Write command. If the Compare operation is not successful, then the Write operation is aborted with a status of Command Aborted due to Failed Fused Command and the contents in the LBA range are not modified. If the Write operation is not successful, the Compare operation completion status is unaffected.

Note: To ensure the Compare and Write is an atomic operation in a multi-host environment, host software should ensure that the size of a Compare and Write fused operation is no larger than the atomic write unit size. Controllers may abort a Compare and Write fused operation that is larger than the atomic write unit size.

Modify the table immediately preceding section 7.5.1.1 as shown below:

Status of IS Register	Pin-based Action	MSI Action
All bits '0' **Note:** May be caused by corresponding bit(s) in the INTM register being set to '1', masking the corresponding interrupt.	Wire inactive	No action
One or more bits set to '1' **Note:** May be caused by corresponding bit(s) in the INTM register being cleared to '0', unmasking the corresponding interrupt.	Wire active	New message sent
One or more bits set to '1', new bit gets set to '1'	Wire active	New message sent
One or more bits set to '1', some (but not all) bits in the IS register are cleared (i.e., host software acknowledges some of the associated completion queue entries)	Wire active	~~No action~~ New message sent
One or more bits set to '1', all bits in the IS register are cleared (i.e., host software acknowledges all associated completion queue entries)	Wire inactive	No action

Modify Figure 50 as shown below:

Figure 50: Firmware Image Download – Command Dword 11

Bit	Description
31:00	**Offset (OFST):** This field indicates the number of Dwords offset from the start of the ~~a 32-bit Dword offset of the~~ firmware image ~~portion~~ being downloaded to the controller. The offset is used to construct the complete firmware image when the firmware is downloaded in multiple pieces. The piece corresponding to the start of the firmware image shall have an Offset of 0h.

Modify the heading of section 5.12.1.12 as shown below:

5.12.1.12 Software Progress Marker (Feature Identifier 80h), (Optional) – NVM Command Set Specific

Modify Figure 73 as shown below:

Figure 73: Set Features – Feature Identifiers

Feature Identifier	O/M	Persistent Across Power States	Uses Memory Buffer for Attributes	Description
00h				Reserved
01h	M	No	No	Arbitration
02h	M	No	No	Power Management
03h	~~M~~ O	Yes	Yes	LBA Range Type
04h	M	No	No	Temperature Threshold
05h	M	No	No	Error Recovery
06h	O	No	No	Volatile Write Cache
07h	M	No	No	Number of Queues
08h	M	No	No	Interrupt Coalescing
09h	M	No	No	Interrupt Vector Configuration
0Ah	M	No	No	Write Atomicity
0Bh	M	No	No	Asynchronous Event Configuration
0Ch – 7Fh				Reserved
80h – BFh				Command Set Specific (Reserved)
C0h – FFh				Vendor Specific

O/M: O = Optional, M = Mandatory

Disposition log

6/5/2012	Erratum captured.
7/16/2012	Erratum ratified.